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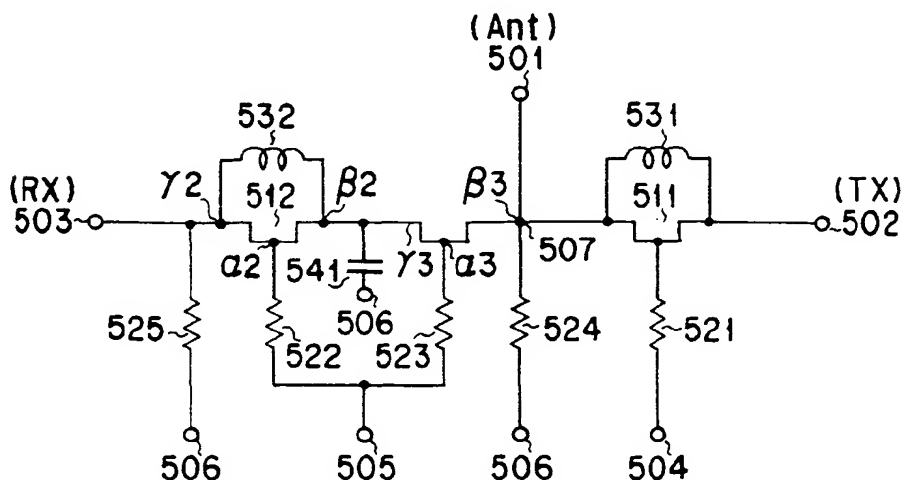
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## switching circuit

switching circuit includes a first transmission input/output terminal (503) connected to one end of the first transmission path, a second input/output terminal (501) connected to the other end of the first transmission path, a second transmission path connected to the second input/output terminal (501), a third input/output terminal (502) connected to the other end of the second transmission path, wherein the second transmission path includes a first field effect transistor.

sistor (512) having a first conduction path which is connected at one end to the first input/output terminal (503), a second field effect transistor (513) having a second conduction path which is connected at one end to the other end of the first conduction path of the first field effect transistor (512) and connected at the other end to the second input/output terminal (501), and a first inductor (532) connected in parallel with the first conduction path of the first field effect transistor (512).



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## Description

This invention relates to a switching circuit for switching high frequency signals.

With miniaturization of communication devices, portable type terminals are rapidly popularized. In order to meet various requirements of the market, various types of communication systems have been developed. In a simple portable telephone system called a PHS (Personal Handy-phone System), in order to reduce the size of the terminal, as shown in FIG. 1, a method using one antenna for switching transmission and reception by use of a high-frequency switch is used. As the high-frequency switch, an SPDT (Single-Pole Dual-Throw) switch is used. Since a weak signal is dealt with on the reception side and a power signal is dealt with on the transmission side, a power loss may sometimes occur in the switch at the transmission time. This problem is specifically explained below.

FIG. 2A is a circuit diagram of a conventional 3-terminal SPDT switching circuit operated on a negative power supply voltage. In the circuit of FIG. 2A, an input/output terminal 101 for high-frequency signal is connected to a signal input/output terminal 102 via a field effect transistor (which is hereinafter referred to as an FET) 111 and the signal input/output terminal 102 is grounded via an FET 113. The signal input/output terminal 101 is connected to a signal input/output terminal 103 via an FET 112 and the signal input/output terminal 103 is grounded via an FET 114. A gate signal input terminal 104 is connected to the gate of the FET 114 via a gate resistor 124 and to the gate of the FET 111 via a gate resistor 121. A gate signal input terminal 105 is connected to the gate of the FET 113 via a gate resistor 123 and to the gate of the FET 112 via a gate resistor 122. The gate resistors 121 to 124 have high resistances of several k $\Omega$ . The FETs 111 to 114 are depletion type FETs. For example, in a switching circuit for switching the state of the antenna of a digital cordless telephone to the transmission state or reception state, the signal input/output terminal 101 is used as the antenna signal terminal, the signal input/output terminal 102 is used as the terminal of the power transmission path on the transmission side, and the signal input/output terminal 103 is used as the terminal of the small signal transmission path on the reception side.

Next, the operation of the above switching circuit is explained. If 0V is applied to the gate signal input terminal 104 and -3V is applied to the gate signal input terminal 105, the FETs 111 and 114 are both turned ON and the FETs 112 and 113 are both turned OFF. If a high-frequency signal is input from the signal input/output terminal 102, it is supplied to the signal input/output terminal 101 via the FET 111. At this time, the signal input from the signal input/output terminal 102 is influenced by the loss caused by the ON-resistance of the FET 111 and the capacitance of the FET 113 in the OFF state and the loss caused by the leakage due to the capaci-

tance of the FET 112 in the OFF state and a signal obtained by subtracting the losses is output from the signal input/output terminal 101. Further, even if a current leaking via the capacitor of the FET 112 in the OFF state between the input/output terminals 101 and 103 on the OFF side, the current flows into the ground via the FET 114 in the ON state and thus high isolation can be attained.

While FIG. 2A shows an example of the conventional SPDT switch operated on 0V and a negative power supply voltage of 3V, FIG. 2B is a circuit diagram showing a conventional SPDT switching circuit operated on 0V and a positive power supply voltage of 3V. The switching circuit of FIG. 2B includes DC-cut capacitors 231 to 233 of several pF respectively connected between the respective input/output terminals 101 to 103 and connection nodes 107 to 109 in the switching circuit of FIG. 2A, a decoupling capacitor 234 of several pF connected between a connection node 210 and the GND terminal, and pull-up resistors 225 and 226 of several k $\Omega$  connected between the power supply terminal 206 and the connection nodes 107 and 210. With the above construction, the switching voltage is raised to the reference potential 3V. The operation of the above switching circuit is basically the same as the SPDT switching circuit operated on the negative power supply voltage and is different in that the reference potential is a positive potential of 3V.

In the above high-frequency switch, for example, in a switch for switching the state of the antenna of a digital cordless telephone to the transmission state or reception state, the signal input/output terminal 102 is used as the terminal of the power transmission path on the transmission side, and the signal input/output terminal 103 is used as the terminal of the small signal transmission path on the reception side. At this time, when a signal input from the terminal 102 is supplied to the antenna terminal 101 via the ON-resistor of the FET 111, the signal is influenced by the loss caused by the capacitance of the FET 113 in the OFF state and the loss caused by the leakage current due to the capacitance of the FET 112 in the OFF state and the loss caused in a region from the terminal 102 on the transmission side to the antenna terminal 101 is increased.

When the functions of the FETs 113 and 114 connected in parallel with the respective transmission paths are considered, the FET 114 has a function of causing a current leaking via the capacitor of the FET 112 connected in series with the transmission path and set in the OFF state to flow into the GND terminal, thus attaining high isolation, but in this case, since the signal passes the capacitor of the FET 113 in the OFF state, the loss is increased.

Further, in the case of the SPDT switch operated on 0V and the positive power supply voltage of 3V shown in FIG. 2B, it is necessary to add the decoupling capacitor 234 of several pF between the connection node 210 and the GND terminal, the layout area becomes large if

circuit is realized by use of a monolithic microwave (MMIC). Further, since the circuit construction is different in the cases of positive power supply and negative power supply, the MMIC chip cannot be commonly therefor. In addition, use of the FETs and 114 connected in parallel with the respective transmission paths causes problems when it is required to reduce the loss, reduce the number of elements and increase the flexibility of the MMIC chip.

An object of this invention is to provide a switching circuit having a high withstand voltage and capable of transmitting a linear output even when a large electric power is transmitted.

In order to attain the above object, a switching circuit according to this invention comprises a first transmission path; a first input/output terminal connected to one end of the first transmission path; a second input/output terminal connected to the other end of the first transmission path; a second transmission path connected to one end to the second input/output terminal; and a third input/output terminal connected to the other end of the second transmission path; wherein the first transmission path includes a first field effect transistor having a first conduction path which is connected at one end to the first input/output terminal; a second field effect transistor having a second conduction path which is connected at one end to the other end of the first conduction path of the first field effect transistor and connected at the other end to the second input/output terminal; and an inductor connected in parallel with the first conduction path of the first field effect transistor.

Further, the second transmission path preferably includes a third field effect transistor having a third conduction path which is connected between the second input/output terminal; and a second inductor connected in parallel with the third conduction path. The capacitance which the first field effect transistor has in an OFF state and the first inductor preferably form a resonance at a preset frequency of the high-frequency signals.

The capacitance which the third field effect transistor has in an OFF state and the second inductor preferably form a resonance at a preset frequency of the high-frequency signals.

The switching circuit can be used to switch high-frequency signals of reception and transmission with the first input/output terminal connected to a reception circuit, the second input/output terminal connected to an antenna, and the third input/output terminal connected to a transmission circuit.

Further, the second input/output terminal is coupled to a reference potential via a resistor, and a preset voltage is preferably applied to gate electrodes of the first and second field effect transistors via respective preset resistors so as to control conduction states of the first and second conduction paths, respectively.

The first and the second transistor is preferably a depletion type transistor.

Further, the second input/output terminal is coupled to a reference potential via a resistor, and a preset voltage is preferably applied to the gate electrode of the third field effect transistor via a preset resistor so as to control a conduction state of the third conduction path.

The third transistor is preferably a depletion type transistor.

The switching circuit preferably comprises a voltage terminal to which a preset voltage is applied and a capacitor connected between the other end of the first conduction path of the first transistor and the voltage terminal.

It is also possible to use a multi-finger type field effect transistor having a plurality of gate electrodes connected to one another as the second field effect transistor.

A gate width of the second field effect transistor is preferably made smaller than a gate width of the first field effect transistor.

When the second transistor is a multi-finger type transistor, a total gate width of a plurality of gate electrodes of the second transistor is preferably made smaller than a gate width of the first transistor.

The switching circuit may further comprise a voltage terminal to which a preset voltage is applied and a fourth transistor having a fourth conduction path connected between the other end of the first conduction path of the first transistor and the voltage terminal to which the preset voltage is applied.

According to this invention, with a construction made by serially connecting two or more field effect transistors (FETs) (or Dual-gate or cascode-connected FET) as a field effect transistor connected in series with the small-signal transmission path (reception path), a voltage applied to each of the FETs in the OFF state can be lowered by voltage division. As a result, the high withstand voltage of the transmission path can be attained and a linear output can be obtained even when a large electric power is transmitted.

While the FET connected in series with the small-signal transmission path is constructed by the two-stage series-connected FETs, the low loss, high isolation, small number of elements, and the flexibility which are the advantages of the parallel resonance type switch can be maintained.

Further, since the capacitor is connected to the connection node of the first and second FETs and the impedance associated with the second FET becomes substantially equal to the impedance associated with the first FET having the inductor for parallel resonance, the voltages applied between the sources and drains of the FETs can be adequately divided. Therefore, when a large signal is input, the OFF state of the FET can be maintained in the more preferable condition and the linear characteristic can be further enhanced.

Since the gate width of the second FET (the total gate width in the case of multi-finger type) connected in the path in which the transmission signal power is rela-

tively small is made smaller than the gate width of the first FET having the inductor for parallel resonance, the voltage applied to the FET can be adequately divided. Therefore, even when a large signal is input, the FET can be adequately kept in the OFF state and the linear characteristic can be further enhanced.

By additionally using the fourth FET having the drain connected to the node of the drain of the first FET and the source of the second FET, the voltage applied between the sources and drains of the first and second FETs can be adequately divided, and therefore, when a large signal is input, the FET can be adequately kept in the OFF state and the linear characteristic can be attained without being influenced by variations in the transistor characteristics caused in the manufacturing process. As a result, the manufacturing yield of the switches can be enhanced.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a general PHS portable telephone;

FIGS. 2A and 2B are circuit diagrams of a conventional high-frequency switch, FIG. 2A showing the case of negative power supply voltage operation and FIG. 2B showing the case of positive power supply voltage operation;

FIG. 3 is a circuit diagram for illustrating a parallel resonance type switching circuit devised by the inventors of this application;

FIGS. 4A to 4E are voltage waveform diagrams showing voltages on nodes or between nodes in the circuit shown in FIG. 3A on the same time base;

FIG. 5 is a circuit diagram of a parallel resonance type switching circuit according to a first embodiment of this invention;

FIGS. 6A to 6I are voltage waveform diagrams showing voltages on nodes or between nodes in the circuit shown in FIG. 5 on the same time base;

FIG. 7 is a diagram showing the relation between the second order distortion and the input power in the first embodiment of this invention;

FIG. 8 is a view showing the layout pattern obtained when the first embodiment is applied to an MMIC;

FIG. 9 is a circuit diagram of a parallel resonance type switching circuit according to a second embodiment of this invention;

FIGS. 10A to 10I are voltage waveform diagrams showing voltages on nodes or between nodes in the circuit shown in FIG. 9 on the same time base;

FIG. 11 is a view showing the layout pattern obtained when the second embodiment is applied to an MMIC;

FIGS. 12A and 12B are diagrams for illustrating the linear characteristic of this invention, FIG. 12A showing the case of the second embodiment and FIG. 12B showing the case of a comparative sample

based on the circuit shown in FIG. 3 on the same time base;

FIGS. 13A and 13B are diagrams for illustrating the characteristic of the second embodiment, FIG. 13A showing the input/output characteristic and FIG. 13B showing the relation between the second order distortion and the input power;

FIG. 14 is a circuit diagram of a parallel resonance type switching circuit according to a third embodiment of this invention;

FIGS. 15A to 15I are voltage waveform diagrams showing voltages on nodes or between nodes in the circuit shown in FIG. 14 on the same time base;

FIG. 16 is a diagram showing the relation between the second order distortion and the input power;

FIG. 17 is a circuit diagram of a high-frequency switch according to a third embodiment of this invention; and

FIG. 18 is a diagram showing the relation between the second order distortion and the input power.

Before explaining the embodiment of this invention, the parallel resonance type switching circuit devised by the inventors of this application is explained. As shown in FIG. 3, in the circuit, the FETs 113 and 114 connected in parallel with the respective transmission paths as is observed in the conventional SPDT switching circuit (for example, FIGS. 2A and 2B) are not used. Further, in this circuit, inductors 331 and 332 which resonate with capacitors of OFF-state FETs 312 and 311 connected in series with the respective transmission paths are connected between the source electrodes and drain electrodes of the respective FETs 312 and 311, a power supply terminal 306 for setting a reference potential is connected to a connection node 307 of the FETs 311 and 312 via a high-resistance resistor, and control voltages are applied to the gates of the FETs via high-resistance resistors.

The impedances of the respective transmission paths in a case wherein the FETs 311 and 312 connected in series with the transmission paths are set in the OFF state become extremely large since the inductors 331 and 332 and the capacitors of the OFF-state FETs 312 and 311 resonate in a preset frequency range. Therefore, currents leaking through the capacitors of the OFF-state FETs can be reduced and the FETs 113 and 114 which are conventionally connected in parallel with the respective transmission paths can be omitted. By omitting the FETs 113 and 114 which are connected in parallel with the respective transmission paths, high isolation can be attained, the loss can be reduced and the number of elements used can be reduced.

When the switch is embodied in a form of an MMIC and if a DC-cut capacitor is attached to the external portion of the MMIC, the circuit on the MMIC can be formed with exactly the same construction for the positive power supply and for the negative power supply and thus an MMIC chip with high flexibility can be obtained.

However, the above circuit has a problem that a linear output cannot be obtained and the signal is distorted when a large signal is input. For example, when a signal is input via the terminal 302 on the transmission side and supplied to the antenna terminal 301 via the ON-state FET 311, the signal is distorted. Voltages of the gate electrode and the source or drain electrode of the FET 312 in the OFF state are influenced by the input signal via the coupling capacitors Cgs, Cgd and Cds of the FET and each of the amplitudes thereof becomes an AC amplitude dependent on the input amplitude, and if the amplitude exceeds the threshold voltage of the FET 312, the FET 312 which is set in the OFF state will be turned ON in AC terms. As a result, the waveform of the signal is distorted and the second order distortion and third order distortion other than the fundamental wave are generated and may cause interference waves.

In the above circuit, the relation between the input power (which is referred to as  $P_{in}$ ) from the power amplifier circuit side and the second order distortion (which is referred to as  $2f_o$ ) when the gate width  $W_g$  of each of the FETs 311 and 312 was set to 1 mm,  $V_{th}$  was set to 1.0V,  $L$  of each of the inductors 331 and 332 was set to 15.5 nH, and  $R$  of each of the gate resistors 321, 322 and 323 was set to 10 k $\Omega$  was checked. The insertion loss at the time of input of a small signal became 0.4 dB at a frequency of 1.9 GHz and the isolation was -35 dB. In the range of  $P_{in}$  from 0 to 18 dBm,  $2f_o$  monotonously increases but  $2f_o$  rapidly increases after  $P_{in}$  becomes larger than 18 dBm.

The monitoring result of the potential concerning the electrode of the FET 12 set in the OFF state is shown in FIGS. 4A to 4E. The nodes  $\alpha$ ,  $\beta$ , and  $\gamma$  are defined as shown in FIG. 3 and variations in the potentials over time on the respective nodes when the input power  $P_{in}$  is set to 19 dBm are shown in FIGS. 4A to 4C on the same time base. If the maximum potentials of the respective nodes (electrodes) are set to  $V_\alpha$ ,  $V_\beta$ , and  $V_\gamma$ , then  $V_\beta = 2.8V$  (amplitude  $\Delta V = 2.8V$ , the same representation is used after this),  $V_\alpha = -0.9V$  ( $\Delta V = 1.8V$ ), and  $V_\gamma = 0V$  ( $\Delta V = 0V$ ).

Therefore, in this case, the voltages between the electrodes of the FET 312 are set such that  $V_{\gamma\beta} = 2.8V$ ,  $V_{\alpha\gamma} = -0.9V$  and  $V_{\alpha\beta} = -1.7V$  as shown in FIGS. 4C to 4E. Since  $V_{\alpha\gamma}$  is larger than  $V_{th}$  ( $= -1.0V$ ), the FET 312 is set in the ON state (FIG. 4B). Thus, it is considered that  $2f_o$  is increased because the FET 312 which has been set in the OFF state starts to be turned ON.

For example, the specification determined by the RCR standard in the PHS (Personal Handy-phone System) requires that the maximum input power in which the second distortion is less than -50 dBc (which is represented by  $\max P_{in}@2f_o < -50 \text{ dBc}$ ) be equal to or higher than 21 dBm. In the case of a parallel resonance type switching circuit, the value of  $\max P_{in}@2f_o < -50 \text{ dBc}$  is 18.8 dBm. This value does not satisfy the RCR standard.

Thus, in the parallel resonance type switching cir-

cuit, if the signal input terminal 302 is used as the terminal of a power transmission path on the transmission side and the signal input terminal 303 is used as the terminal of a small signal transmission path on the reception side, there occurs a problem that an input signal is distorted and a linear output cannot be obtained when a large electric power is input to the terminal 302 on the transmission side and the input signal is supplied to the antenna terminal 301 via the FET 311 set in the ON state.

This is because the potentials on the gate electrode (node $\alpha$ ), source electrode (node $\beta$ ), and drain electrode (node $\gamma$ ) of the FET 312 set in the OFF state are influenced by the input signal via the coupling capacitors (Cgs, Cgd, Cds) of the FET and they come to have AC amplitudes dependent on the input amplitude when a large input signal is supplied to the power transmission path on the transmission side, and as a result,  $V_{gs}$  ( $V_{\alpha\beta}$ ) or  $V_{gd}$  ( $V_{\alpha\gamma}$ ) of the FET 312 increases until it exceeds the breakdown voltage (withstand voltage) of the FET.

When the linear output cannot be obtained and, for example, if a switch for selectively switching the antenna of the digital cordless telephone to the transmission or reception state is used, interference waves may be caused as spurious noise and may cause a serious problem.

This invention has been made to solve the above problem and provide a switching circuit capable of attaining a high withstand voltage and obtaining a linear output when a large power is transmitted while maintaining the advantage of the parallel resonance type switching circuit.

There will now be described embodiments of this invention with reference to the accompanying drawings.

(First Embodiment)

FIG. 5 is a circuit diagram of an SPDT switching circuit according to a first embodiment of this invention, and FIGS. 6A to 6I are waveform diagrams showing variations in potentials on nodes or between nodes in the circuit shown in FIG. 5.

In FIG. 5, an input/output terminal 501 for high-frequency signal is connected to an input/output terminal 502 via an FET 511, and the signal input/output terminal 501 is connected to a signal input/output terminal 503 via FETs 512 and 513.

A signal input/output terminal 504 is connected to the gate of the FET 511 via a gate resistor 521. A gate signal input terminal 505 is connected to the gates of the FET 512 and 513 via respective gate resistors 522 and 523.

Inductors 531 and 532 are connected between the source electrodes and drain electrodes of the FETs 511 and 512, respectively. The inductors 531 and 532 construct parallel resonance circuits in cooperation with capacitors of the OFF-state FETs 511 and 512 and are designed to have inductances determined according to the

capacitances of the OFF-state FETs so that the impedances thereof will become maximum at a frequency of 1.9 GHz used for digital cordless telephones.

Further, one end of a capacitor 541 is connected to a connection node of the FETs 512 and 513. A power supply terminal 506 for setting a reference potential is connected to a connection node 507 of the FETs 511 and 513 via a high-resistance resistor 524 and connected to the signal input/output terminal 503 via a high-resistance resistor 525. The FETs 511, 512 and 513 are depletion type FETs.

A case wherein the signal input/output terminal 501 is used as an antenna signal terminal Ant, the signal input/output terminal 502 is used as a terminal Tx of the power transmission path on the transmission side, and the signal input/output terminal 503 is used as a terminal Rx of the small-signal transmission path on the reception side is considered.

When 0V is applied to the gate signal input terminal 504, -2.7V is applied to the gate signal input terminal 505 and 0V is applied to the power supply terminal 506, then the FET 511 is turned ON, the FETs 512 and 513 are turned OFF, and a signal input from the terminal Tx on the transmission side is supplied to the antenna signal terminal Ant via the ON resistor of the FET 511.

Next, the elements are explained. The gate widths  $W_g$  of the FETs 511 and 512 are all set to 1 mm, the gate width  $W_g$  of the FET 513 is set to 400  $\mu\text{m}$ , and the threshold voltages  $V_{th}$  thereof are all set to -1.0V. The FET is a multi-finger type FET (which is comprised of series-connected unit transistors), each unit transistor having a unit gate width of 100  $\mu\text{m}$ .

The inductors 531 and 532 are rectangular spiral inductors, each having inductance  $L$  of 15.5 nH, a line width of 10  $\mu\text{m}$ , a space of 5  $\mu\text{m}$ , a film thickness of 3  $\mu\text{m}$ , and a one-side length of 340  $\mu\text{m}$ . The resistance  $R$  of each of the gate resistors 521, 522, 523, 524 and 525 is 10 k $\Omega$  and the capacitance of the capacitor 541 is 0.5 pF.

In this embodiment, by connecting the capacitor 541 to the connection node of the first FET 512 and the second FET 513, the impedance of the second FET 513 can be made equal to the impedance of the first FET 512 having the inductor for parallel resonance and an adequately divided voltage can be applied to the single FET. Therefore, the OFF state of the FET can be stably maintained when a large signal is input and the linear characteristic at the time of large power input can be further enhanced.

The monitoring results of the potentials of the respective electrodes (nodes) in this embodiment are shown in FIGS. 6A to 6I on the same time base. In this circuit, a high-frequency power input to the Tx terminal 502 is set to  $P_{in} = 22$  dBm. The maximum potentials of the respective electrodes are set to  $V_{\Delta 3} = 4.0\text{V}$  (amplitude  $\Delta V = 4.0\text{V}$ ),  $V_{\alpha 3} = 0.3\text{V}$  ( $\Delta V = 3.0\text{V}$ ),  $V_{\gamma 3} = v_{\beta 2} = 2.2\text{V}$  ( $\Delta V = 2.2\text{V}$ ),  $V_{\alpha 2} = -1.2\text{V}$  ( $\Delta V = 1.5\text{V}$ ), and  $V_{\gamma 2} = 0\text{V}$  ( $\Delta V = 0\text{V}$ ).

Therefore, in the FET 513,  $v_{\beta 3\gamma 3} = 1.8\text{V}$ ,  $V_{\alpha 3\gamma 3} = -1.9\text{V}$  and  $V_{\alpha 3\beta 3} = -3.7\text{V}$ , and in the FET 512,  $v_{\beta 2\gamma 2} = 2.2\text{V}$ ,  $V_{\alpha 2\gamma 2} = -1.2\text{V}$  and  $V_{\gamma 2\beta 2} = -2.2\text{V}$ . The FETs 512 and 513 are set in the OFF state.

The relation between  $P_{in}$  and  $2f_o$  of a switch formed in the above condition is indicated by  $\Delta$  marks in FIG. 7. The same relation of the parallel resonance type switch described prior to the explanation of the embodiment as a comparative sample is indicated by  $\circ$  marks. The abscissa indicates  $P_{in}$  and the ordinate indicates  $2f_o$ .

According to this embodiment,  $2f_o$  monotonously increases while  $P_{in}$  is set in a range of 0 to 24.5 dBm, but when  $P_{in}$  exceeds 26 dBm,  $2f_o$  rapidly increases and the value of ( $\max P_{in} @ 2f_o < -50$  dBc) is 28.5 dBm. This value has a sufficiently large margin with respect to the RCR standard ( $\max P_{in} @ 2f_o < -50$  dBc  $\geq 21$  dBm) and produces no practical problem.

$3f_o$  rapidly increases after  $P_{in}$  exceeds 25 dBm. The insertion loss at the time of small signal input is 0.38 dB at a frequency of 1.9 GHz and the isolation is -40 dB.

In this embodiment,  $V_{\alpha 2\gamma 2}$  of the FET 512 is as small as -1.6V and the FET can maintain the OFF state.

Further, in the insertion loss and isolation in this embodiment, the insertion loss is 0.38 dB at a frequency of 1.9 GHz and the isolation is -40 dB, and thus a preferable result can be obtained.

FIG. 8 shows the layout pattern of the MMIC switch. The reference numerals used in FIG. 8 correspond to those of FIG. 5. In the right side portion, the terminal 502 of the power transmission path on the transmission side is provided, in the left side portion, the terminal 503 of the small signal transmission path on the reception side is provided, in the central lower portion, the antenna terminal 501 and power supply terminal 506 are provided, and in the central upper portion, the gate signal input terminal 505 is provided. Further, in the right side portion, the inductor 531 used for the power transmission path is arranged, and in the left side portion, the inductor 532 used for the small signal transmission path is arranged. In addition, the FET 511 used for the power transmission path is arranged in the right side portion and the FETs 512 and 513 used for the power transmission path are arranged in the central and left side portions. In order to prevent the interference between the two inductors, a GND plane is provided therebetween. The chip size is 1.1 mm  $\times$  1.0 mm.

In this embodiment, the resistors 521, 522, 523, 524 and 525 are used in lines through which the DC power supply voltage is supplied, but the purpose of using the resistors is to cut off the RF signal component in the DC power and it is possible to use inductors to serve the same purpose.

Further, in this invention, the second transmission path via which a larger power than in the first transmission path is passed can be formed with a conventional construction of an FET and a resistor other than the construction of the third FET 511 and the inductor 531.

(Second Embodiment)

FIG. 9 is a circuit diagram of a switching circuit according to a second embodiment of this invention, and FIGS. 10A to 10I are waveform diagrams showing variations in potentials over time on nodes or between nodes in the circuit shown in FIG. 9 on the same time base. In FIGS. 10A to 10I, solid lines show the waveforms at  $P_{in}=19$  dBm, and broken lines show waveforms at  $P_{in}=22$  dBm.

An input/output terminal 601 for high-frequency signal is connected to an input/output terminal 602 via an FET 611 and connected to a signal input/output terminal 603 via FETs 612 and 613. The FETs 612 and 613 used for the small signal transmission path are serially connected.

A gate signal input terminal 604 is connected to the gate of the FET 611 via a gate resistor 621. A gate signal input terminal 605 is connected to the gates of the FETs 612 and 613 via gate resistors 622 and 623, respectively.

Inductors 631 and 632 are connected between the drain electrodes and source electrodes of the FETs 611 and 612, respectively. The inductors 631 and 632 construct parallel resonance circuits in cooperation with the capacitors of the OFF-state FETs 611 and 612 and the inductances thereof are determined to adequate values according to the capacitances of the OFF-state FETs so that the impedances thereof will become maximum at a frequency of 1.9 GHz used for digital cordless telephones, for example.

A power supply terminal 606 for setting the reference potential is connected to a connection node 607 of the FETs 611 and 613 via a high-resistance resistor 624. The FETs 611, 612 and 613 are depletion type FETs.

FIG. 11 is a layout view of an MMIC having the above circuit actually formed on a chip.

The operation of the above switch effected in a case wherein the signal input/output terminal 601 is used as an antenna signal terminal Ant, the signal input/output terminal 602 is used as a terminal Tx of the power transmission path on the transmission side, and the signal input/output terminal 603 is used as a terminal Rx of the small-signal transmission path on the reception side is explained.

When 0V is applied to the gate signal input terminal 604, -2.7V is applied to the gate signal input terminal 605 and 0V is applied to the power supply terminal 606, then the FET 611 is turned ON and the FETs 612 and 613 are turned OFF. When a signal input from the terminal Tx on the transmission side is supplied to the antenna signal terminal Ant via the ON resistor of the FET 611, a signal obtained by subtracting the influence by the loss of leakage current into the small signal transmission path on the OFF side and the ON resistor of the FET 611 from the input signal is supplied to the antenna terminal Ant.

The leakage of the signal into the small signal transmission path on the OFF side is determined by the ratio of the impedance  $Z$  of the small signal transmission path on the OFF side to the resistance of a  $50\Omega$  terminal resistor connected to the antenna terminal Ant. As the impedance  $Z$  of the small signal transmission path on the OFF side is larger, the loss of insertion from the terminal Tx on the transmission side into the antenna terminal Ant is reduced.

The results of comparison by simulation of the linear characteristic of the parallel resonance type high-frequency switch (comparative sample) explained prior to the preferred embodiments with that of the second embodiment are shown in FIGS. 12A and 12B. FIG. 12A shows the waveform in the case of this embodiment and FIG. 12B shows the waveform in the case of the parallel resonance type high-frequency switch of the comparative sample explained prior to the preferred embodiments.

In the above simulation,  $0.6\mu\text{m}$  GaAs MESFETs are used as the FETs 611, 612, 631 and 632 and the gate widths thereof are all set to 1 mm. The power supply voltage is set to 2.7V and the threshold voltages ( $V_{th}$ ) of the FETs are all set to -1V. Further, the resistance of the high-resistance of the resistor is set to  $18k\Omega$ . The inductance of the inductor is set to 15.5 nH.

The input signal is a single tone input of 1.9 GHz and the input power with  $P_{in} = 0$  dBm or  $P_{in} = 21$  dBm is input via Tx. For example, when it is assumed to use a digital cordless telephone, a typical power supplied from the power amplifier is approximately  $P_{in} = 21$  dBm. As shown in FIG. 12B, distortion occurs in the waveform at the time of  $P_{in} = 21$  dBm (D portion). This is because the FET set in the OFF state will be turned ON for AC current. The waveform of FIG. 12A shows a normal waveform. This is obtained based on the effect that the divided voltage is applied to each FET in the case of this invention.

FIG. 13A shows the  $P_{in}$ - $P_{out}$  characteristic. In comparison with a 1-dB compression point ( $P_{1dB}$ ) at which the output is lowered than that of the extrapolation line by 1 dB, it is understood that the linearity can be attained in a range to a point of 23 dB in the case of the high-frequency switch in the prior art and to a point of 33 dB in the case of the high-frequency switch according to the second embodiment of this invention and thus the linear characteristic is improved. Further, the parallel resonance type switching circuit of comparative sample exhibits a characteristic of  $P_{1dB} = 25$  dB.

A second order distortion ( $2f_0$ ) is shown in FIG. 13B as the harmonics distortion. Assuming that the input power is a single tone input of 1.9 GHz and the comparison is made in the case of  $P_{in} = 21$  dBm, the harmonics distortion indicates -35 dBc in the case of the parallel resonance type switching circuit of comparative sample and -60 dBc in the case of the switching circuit of the second embodiment and thus the harmonics distortion is improved. The loss and isolation in the case of the



parallel resonance type switching circuit of comparative sample are respectively 0.4 dB and 35 dB, and the loss and isolation in the case of the second embodiment are 0.4 dB and 36 dB. Therefore, the low loss and high isolation which are the advantages of the parallel resonance type high-frequency switch can be maintained.

According to this embodiment, by connecting FETs of two or more stages in series with the small signal transmission path (or using a Dual-gate or cascode-connected FETs), the effect that the divided voltage is applied to each FET in the small signal transmission path when the FET is turned OFF can be attained. As a result, the transmission path is formed to have a high withstand voltage and a linear output can be obtained even when a larger output is transmitted. Further, the low loss, high isolation, small number of elements and flexibility which are the advantages of the parallel resonance type switch can be maintained and the linear output can be obtained while the FETs connected to the small signal transmission path are formed with 2-stage series construction.

#### (Third Embodiment)

FIG. 14 is a circuit diagram of an SPDT switch according to a third embodiment of this invention and designed for use as an antenna switch in the digital cordless telephone and FIGS. 15A to 15I are waveform diagrams showing variations in potentials on the same time base on nodes or between nodes in the circuit shown in FIG. 14 at Pin = 22 dBm.

In FIG. 14, an input/output terminal 701 for high-frequency signal is connected to an input/output terminal 702 via an FET 711 and connected to a signal input/output terminal 703 via FETs 712 and 713.

A gate signal input terminal 704 is connected to the gate of the FET 711 via a gate resistor 721. A gate signal input terminal 705 is connected to the gates of the FETs 712 and 713 via gate resistors 722 and 723, respectively. Inductors 731 and 732 are connected between the drain electrodes and source electrodes of the FETs 711 and 712, respectively.

The inductors 731 and 732 construct parallel resonance circuits in cooperation with the capacitors of the OFF-state FETs 711 and 712, and the inductances thereof are determined to adequate values according to the capacitances of the OFF-state FETs, so that the impedances thereof will become maximum at a frequency of 1.9 GHz used for digital cordless telephones.

A power supply terminal 706 for applying the reference potential is connected to a connection node 707 of the FETs 711 and 713 via a high-resistance resistor 724 and connected to the signal input/output terminal 703 via a high-resistance resistor 725. The FETs 711, 712 and 713 are depletion type FETs.

A case wherein the signal input/output terminal 701 is used as an antenna signal terminal Ant, the signal input/output terminal 702 is used as a terminal Tx of the power transmission path on the transmission side, and

the signal input/output terminal 703 is used as a terminal Rx of the small-signal transmission path on the reception side is considered.

When 0V is applied to the gate signal input terminal 704, -2.7V is applied to the gate signal input terminal 705 and 0V is applied to the power supply terminal 706, then the FET 711 is turned ON, the FETs 712 and 713 are turned OFF, and a signal input from the terminal Tx on the transmission side is supplied to the antenna signal terminal Ant via the ON resistor of the FET 711.

Next, the elements are explained. The gate widths Wg of the FETs 711 and 712 are all set to 1 mm, the gate width Wg of the FET 713 is set to 400  $\mu$ m, and the threshold voltages Vth thereof are all set to -1.0V. The FET is a multi-finger type FET constructed by a plurality of unit FETs with the unit gate width of 100  $\mu$ m.

The inductors 731 and 732 are rectangular spiral inductors having inductance L of = 15.5 nH, a line width of 10  $\mu$ m, a space of 5  $\mu$ m, a film thickness of 3  $\mu$ m, and a one-side length of 340  $\mu$ m. The resistance R of each of the gate resistors 721, 722, 723, 724 and 725 is 10 k $\Omega$ .

From the monitoring result of the potentials of the respective electrodes in a case of Pin = 22 dB in the circuit of this embodiment effected for comparison with the circuit of the second embodiment in which the gate width Wg is set to 1 mm, the maximum potentials of the respective electrodes (nodes) are set to V $\beta$ 3 = 4.0V (amplitude  $\Delta$ V = 4.0V), V $\alpha$ 3 = 0.3V ( $\Delta$ V = 3.0V), V $\beta$ 3 = 2.2V ( $\Delta$ V = 2.2V), V $\alpha$ 2 = -1.2V ( $\Delta$ V = -1.5V), and V $\gamma$ 2 = 0V ( $\Delta$ V = 0V).

Therefore, in the FET 713, V $\beta$ 3 $\gamma$ 3 = 1.8V, V $\alpha$ 3 $\gamma$ 3 = -1.9V and V $\alpha$ 3 $\gamma$ 3 = -3.7V, and in the FET 712, V $\alpha$ 3 $\gamma$ 2 = 2.2V, V $\alpha$ 2 $\gamma$ 2 = -1.3V, and V $\alpha$ 2 $\gamma$ 3 = -2.2V. The FETs 712 and 713 are set in the OFF state.

On the other hand, in the case of the circuit of the second embodiment (refer to broken lines in FIGS. 10A to 10I), V $\beta$ 3 = 4.0V ( $\Delta$ V = 4.1V), V $\alpha$ 3 = 0.7V ( $\Delta$ V = 3.4V), V $\gamma$ 3 = 2.6V ( $\Delta$ V = 2.6V), V $\alpha$ 2 = -0.7V ( $\Delta$ V = 2.0V), and V $\gamma$ 2 = 0V ( $\Delta$ V = 0V). In comparison with the second embodiment, in this embodiment, it is understood that the amplitudes of the voltages on the respective nodes in the FET 712 are reduced and the FET is difficult to be turned ON. This is considered to be because the gate width of the FET 713 is reduced to reduce the coupling capacitance and the power from the ON side is difficult to leak through the FET 713 so as to reduce the amplitudes of the potentials on the respective nodes.

In this embodiment, as shown in FIG. 16, the value of (maxPin@2fo<-50 dBc) is 24.5 dBm and the RCR standard can be satisfied with large margin by making the gate width of the FET 713 series-connected with the FET 712 smaller than the gate width of the FET 712.

Further, in this embodiment, the insertion loss at a frequency of 1.9 GHz is 0.35 dB and the isolation is -38 dB and this is considered to be because the impedance on the OFF side is further increased by reducing the gate width of the FET 713.



(Fourth Embodiment)

FIG. 17 is a circuit diagram of an SPDT switch according to a fourth embodiment of this invention. In FIG. 17, an input/output terminal 801 for high-frequency signal is connected to an input/output terminal 802 via an FET 811 and connected to a signal input/output terminal 803 via FETs 812 and 813.

A gate signal input terminal 804 is connected to the gate of the FET 811 via a gate resistor 821. A gate signal input terminal 805 is connected to the gates of the FETs 812 and 813 via gate resistors 822 and 823, respectively. Inductors 831 and 832 are connected between the drain electrodes and source electrodes of the FETs 811 and 812, respectively.

The inductors 831 and 832 construct parallel resonance circuits in cooperation with the capacitors of the OFF-state FETs 811 and 812, and the inductances thereof are determined to adequate values according to the capacitances of the OFF-state FETs, so that the impedances thereof will become maximum at a frequency of 1.9 GHz used for digital cordless telephones.

A power supply terminal 806 for applying a first reference potential is connected to a connection node 807 of the FETs 811 and 813 via a high-resistance resistor 824, connected to the signal input/output terminal 803 via a high-resistance resistor 825 and connected to the source electrode (or drain electrode) of the FET 814 via a high-resistance resistor 826.

Further, a power supply terminal 808 for applying a second reference potential is connected to the gate of the FET 814 via a high-resistance resistor 827. The FETs 811, 812, 813 and 814 are depletion type FETs.

A case wherein the signal input/output terminal 801 is used as an antenna signal terminal Ant, the signal input/output terminal 802 is used as a terminal Tx of the power transmission path on the transmission side, and the signal input/output terminal 803 is used as a terminal Rx of the small-signal transmission path on the reception side is considered.

When 0V is applied to the gate signal input terminal 804, -2.7V is applied to the gate signal input terminal 805, 0V is applied to the power supply terminal 806 and -2.7V is applied to the power supply terminal 808, then the FET 811 is turned ON, the FETs 812, 813 and 814 are turned OFF, and a signal input from the terminal Tx on the transmission side is supplied to the antenna signal terminal Ant via the ON resistor of the FET 811.

Next, the elements are explained. The gate widths  $W_g$  of the FETs 811, 812, 813 and 814 are all set to 1 mm, and the threshold voltages  $V_{th}$  thereof are all set to -1.0V. The FET is a multi-finger type FET constructed by a plurality of unit FETs with the unit gate width of 100  $\mu$ m.

The inductors 831 and 832 are rectangular spiral inductors, each having inductance  $L$  of 15.5 nH, a line width of 10  $\Omega$ m, a space of 5  $\mu$ m, a film thickness of 3  $\mu$ m, and a one-side length of 340  $\mu$ m. The resistance  $R$

of each of the gate resistors 821, 822, 823, 824, 825, 826 and 827 is set to 10 k $\Omega$ .

The relation between  $P_{in}$  and  $2f_o$  of a switch formed in the above condition is shown in FIG. 18. In this embodiment, the value of  $(\max P_{in} @ 2f_o < -50 \text{ dBc})$  is 30.0 dBm and is improved over that of the switching circuit of the first embodiment by 1.0 dBm. This is because the capacitance of the capacitor 506 is deviated from the capacitance of the OFF-state FET 513 and  $V_{ds}$  of the FET 513 is made slightly different from  $V_{ds}$  of the FET 512 in the case of the switching circuit of the first embodiment, but in this embodiment, the capacitances of the OFF-state FETs 813 and 814 are substantially equal to each other, the voltage can be adequately divided and  $V_{ds}$  of the FET 813 is equal to  $V_{ds}$  of the FET 814.

Further, evaluation was made by supplying 100 wafers (100 chips/wafers) and it was found that the yield in the first embodiment was 60%, but in this embodiment, the yield was enhanced to 80% since the circuit of this embodiment was not influenced by a variation in the FET characteristic in the manufacturing process and the voltage applied between the source and drain of each FET could be adequately divided.

The layout size of this embodiment is substantially the same as that of the first embodiment. In order to prevent the interference between the two inductors, a GND plane is provided between the inductors. The chip size is 1.1 mm  $\times$  1.0 mm.

In this invention, a case wherein the high-resistance resistor is used in a line through which the DC power supply voltage is supplied is explained, but the purpose of using the resistor is to cut off the RF signal component in the DC power, and it is of course possible to use inductors to serve the same purpose.

As described above, according to the switching circuit of this invention, a high withstand voltage can be attained and a sufficiently linear output can be obtained when a larger power is transmitted.

## Claims

### 1. A switching circuit comprising:

- a first transmission path;
  - a first input/output terminal (503, 603, 703, 803) connected to one end of said first transmission path;
  - a second input/output terminal (501, 601, 701, 801) connected to the other end of said first transmission path;
  - a second transmission path connected at one end to said second input/output terminal (501, 601, 701, 801); and
  - a third input/output terminal (502, 602, 702, 802) connected to the other end of said second transmission path;
- wherein said first transmission path includes a

first field effect transistor (512, 612, 712, 812) having a first conduction path which is connected at one end to said first input/output terminal (503, 603, 703, 803); a second field effect transistor (513, 613, 713, 813) having a second conduction path which is connected at one end to the other end of the first conduction path of said first field effect transistor (512, 612, 712, 812) and connected at the other end to said second input/output terminal (501, 601, 701, 801); and a first inductor (532, 632, 732, 832) connected in parallel with the first conduction path of said first field effect transistor (512, 612, 712, 812).

2. A switching circuit according to claim 1, characterized in that said second transmission path includes a third field effect transistor (511, 611, 711, 811) having a third conduction path which is connected between said second and said third (502, 602, 702, 802) input/output terminal; and a second (501, 601, 701, 801) inductor (531, 631, 731, 831) connected in parallel with the third conduction path.
3. A switching circuit according to claim 2, characterized in that said first input/output terminal (503, 603, 703, 803) is connected to a reception circuit, said second input/output terminal (501, 601, 701, 801) is connected to an antenna, and said third input/output terminal (502, 602, 702, 802) is connected to a transmission circuit so as to switch high-frequency signals of reception and transmission.
4. A switching circuit according to claim 3, characterized in that a capacitance which said first field effect transistor (512, 612, 712, 812) has in an OFF state and said first inductor (532, 632, 732, 832) resonate at a preset frequency of the high-frequency signal.
5. A switching circuit according to claim 3, characterized in that a capacitance which said third field effect transistor (511, 611, 711, 811) has in an OFF state and said second inductor (531, 631, 731, 831) resonate at a preset frequency of the high-frequency signals.
6. A switching circuit according to claim 1, characterized in that said second input/output terminal (501, 601, 701, 801) is coupled to a reference potential via a resistor (524, 624, 724, 824), and preset voltages applied to gate electrodes of said first (512, 612, 712, 812) and said second (513, 613, 713, 813) field effect transistors are applied via respective preset resistors (522, 523, 622, 623, 722, 723, 822, 823) to control conduction states of the first and the second conduction path respectively.
7. A switching circuit according to claim 1, character-

ized in that said first (512, 612, 712, 812) and said second (513, 613, 713, 813) transistor is a depletion type transistor.

8. A switching circuit according to claim 2, characterized in that a reference potential is applied to said second input/output terminal (501, 601, 701, 801) via a resistor (524, 624, 724, 824) and a preset voltage is applied to a gate electrode of said third field effect transistor (511, 611, 711, 811) via a preset resistor (521, 621, 721, 821) to control a conduction state of the third conduction path.
9. A switching circuit according to claim 2, characterized in that said third transistor (511, 611, 711, 811) is preferably a depletion type transistor.
10. A switching circuit according to claim 1, characterized by further comprising a voltage terminal (506) to which a preset voltage is applied and a capacitor (541) connected between the other end of the first conduction path of said first transistor (512) and said voltage terminal (506).
11. A switching circuit according to claim 1, characterized in that said second field effect transistor (513, 613, 713, 813) is a multi-finger type field effect transistor having a plurality of gate electrodes connected to one another.
12. A switching circuit according to claim 1, characterized in that a gate width of said second field effect transistor (513, 613, 713, 813) is smaller than a gate width of said first field effect transistor (512, 612, 712, 812).
13. A switching circuit according to claim 11, characterized in that a total gate width of a plurality of gate electrodes of said second field effect transistor (513, 613, 713, 813) is smaller than a gate width of said first field effect transistor (512, 612, 712, 812).
14. A switching circuit according to claim 1, characterized by further comprising a voltage terminal (806) to which a preset voltage is applied and a fourth transistor (814) having a fourth conduction path connected between the other end of the first conduction path of said first transistor (812) and said voltage terminal (806) to which the preset voltage is applied.
15. A switching circuit comprising:
  - a first input/output terminal (503, 603, 703, 803);
  - a first field effect transistor (512, 612, 712, 812) having a first source electrode connected to said first input/output terminal (503, 603, 703,

- 803), a first drain electrode and a first gate electrode;  
 a first inductor (532, 632, 732, 832) connected between the first source electrode and the first drain electrode;  
 a second field effect transistor (513, 613, 713, 813) having a second source electrode connected to the first drain electrode, a second drain electrode and a second gate electrode;  
 a first control terminal (505, 605, 705, 805) for controlling conduction states of said first (512, 612, 712, 812) and said second (513, 613, 713, 813) field effect transistor;  
 a first resistor (522, 622, 722, 822) connected between said first control terminal (505, 605, 705, 805) and the first gate electrode;  
 a second resistor (523, 623, 723, 823) connected between said first control terminal (505, 605, 705, 805) and the second gate electrode;  
 a second input/output terminal (501, 601, 701, 801) connected to the second drain electrode;  
 a first voltage terminal (506, 606, 706, 806) for applying a reference potential;  
 a third resistor (524, 624, 724, 824) connected between said voltage terminal (506, 606, 706, 806) and said second input/output terminal (501, 601, 701, 801);  
 a third field effect transistor (511, 611, 711, 811) having a third source electrode connected to said second input/output terminal (501, 601, 701, 801), a third drain electrode and a third gate electrode;  
 a second inductor (531, 631, 731, 831) connected between the third source electrode and the third drain electrode;  
 a third input/output terminal (502, 602, 702, 802) connected to the third drain electrode;  
 a second control terminal (504, 604, 704, 804) for controlling a conduction state of said third field effect transistor (511, 611, 711, 811); and  
 a fourth resistor (521, 621, 721, 821) connected between said second control terminal (504, 604, 704, 804) and the third gate electrode.
16. A switching circuit according to claim 15, characterized by further comprising a second voltage terminal (506) for applying a preset voltage and a capacitor (541) connected between the first drain electrode and said second voltage terminal (506).
17. A switching circuit according to claim 15, characterized in that said second field effect transistor (513, 613, 713, 813) is a multi-finger type field effect transistor having a plurality of gate electrodes connected to one another.
18. A switching circuit according to claim 15, characterized in that a gate width of said second field effect

transistor (513, 613, 713, 813) is smaller than a gate width of said first field effect transistor (512, 612, 712, 812).

19. A switching circuit according to claim 17, characterized in that a total gate width of a plurality of gate electrodes of said second field effect transistor (513, 613, 713, 813) is smaller than a gate width of said first field effect transistor (512, 612, 712, 812).
20. A switching circuit according to claim 15, characterized by further comprising a third voltage terminal (806) for applying a preset voltage and a fourth field effect transistor (814) having a fourth source electrode connected to said third voltage terminal (806), a fourth drain electrode connected to the first drain electrode, and a fourth gate electrode.

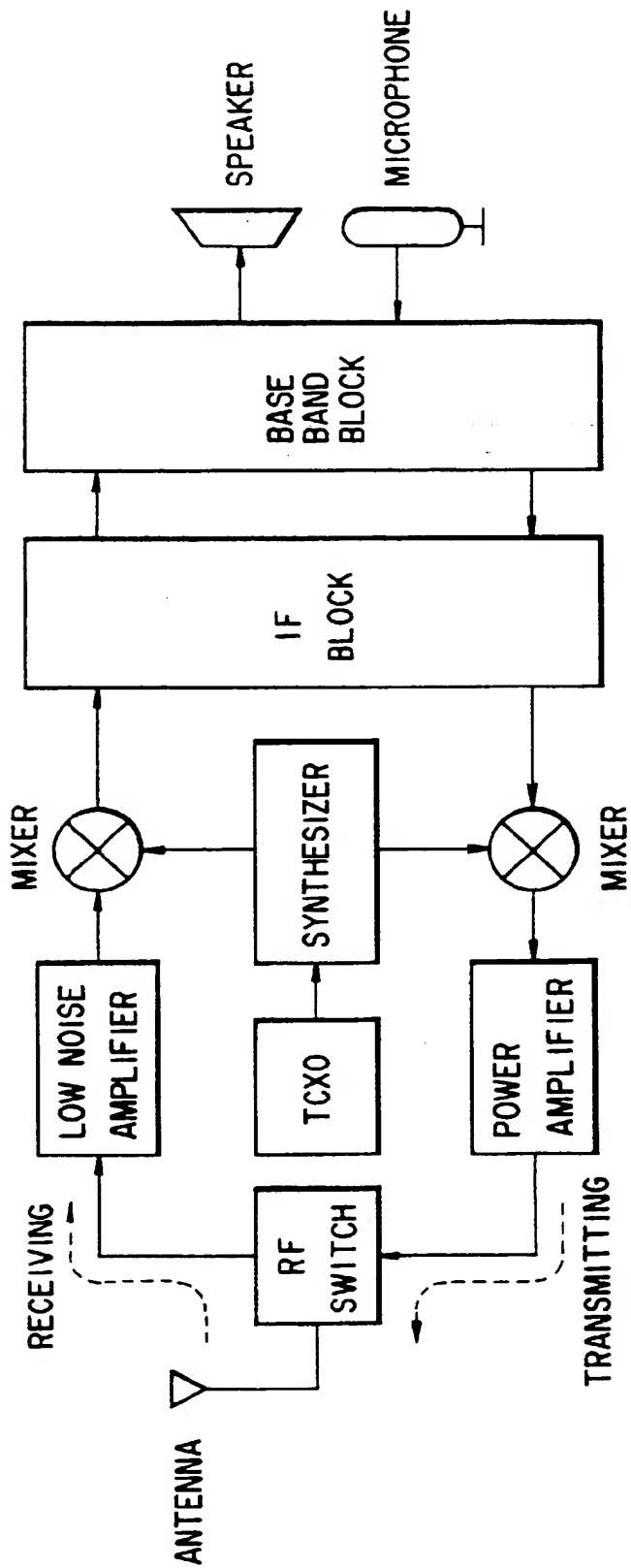


FIG. 1

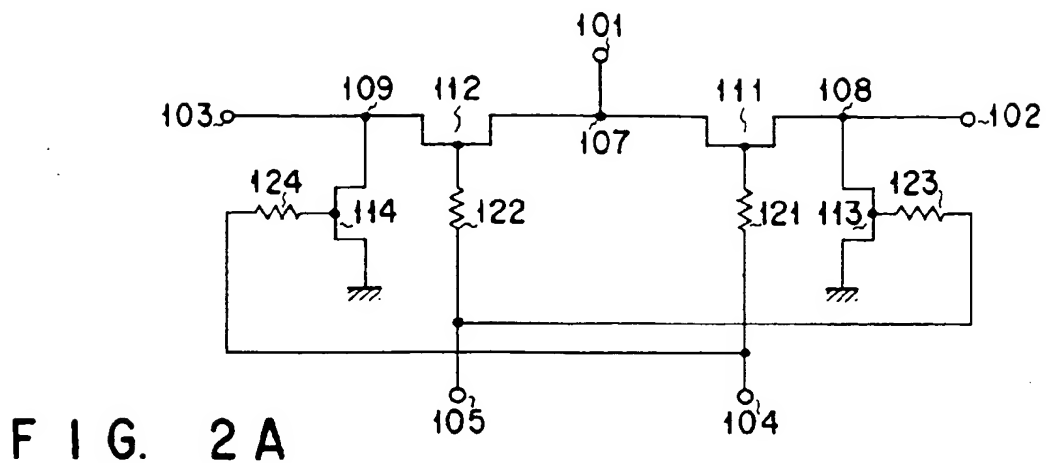


FIG. 2A

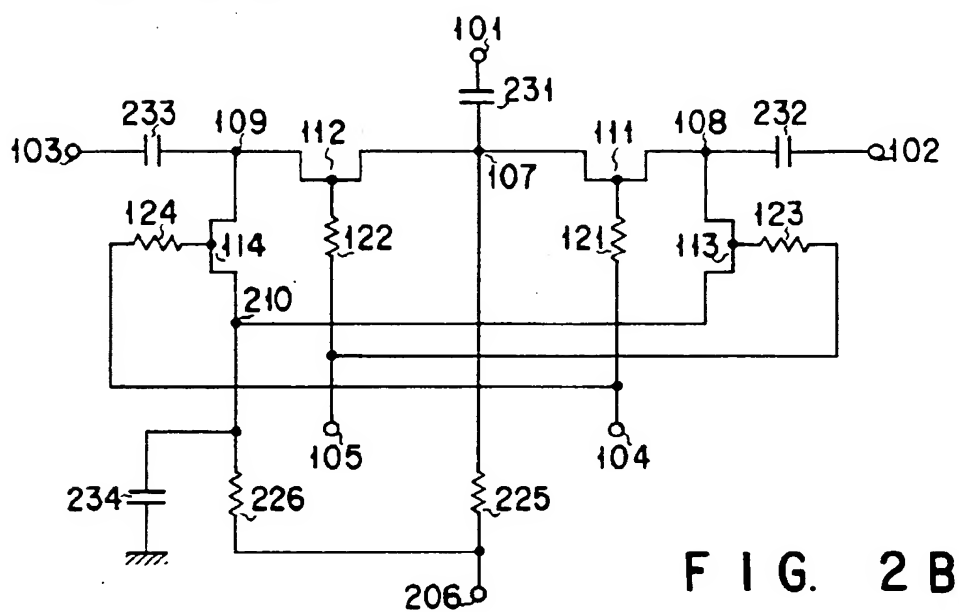


FIG. 2B

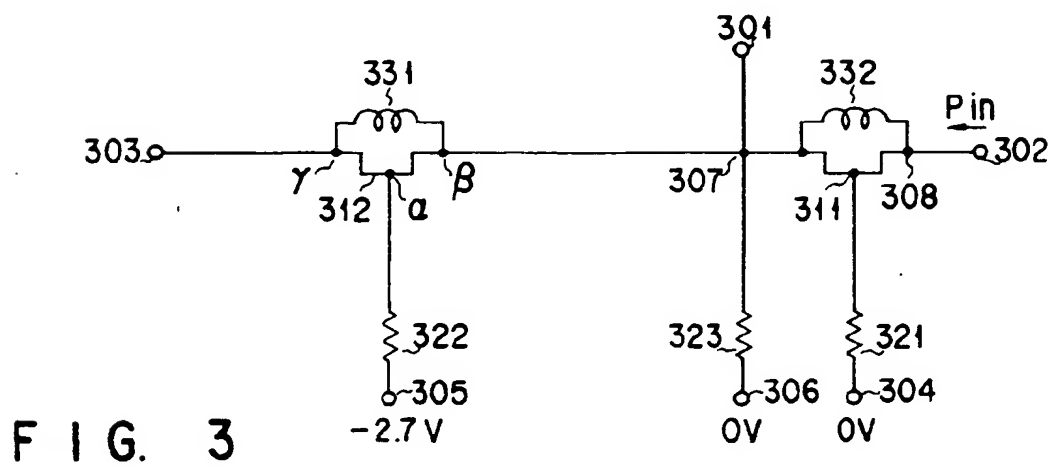
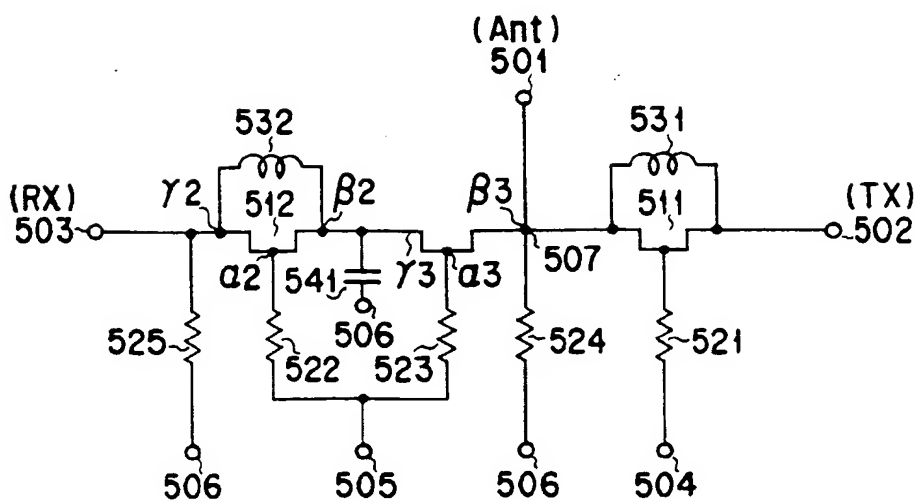
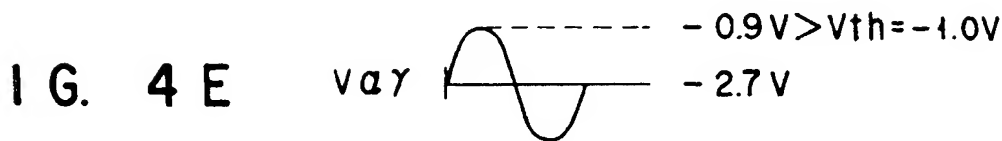
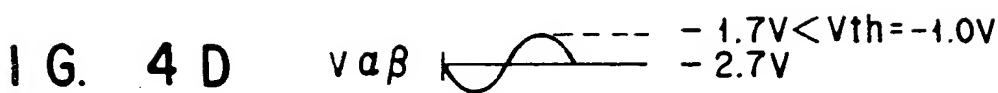
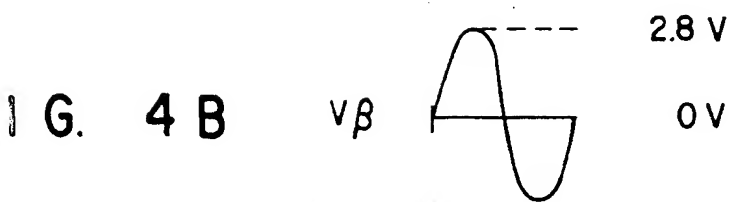
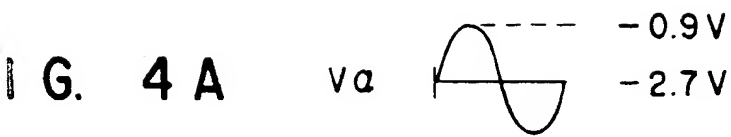


FIG. 3



I G. 5

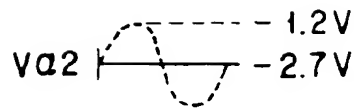


FIG. 6A

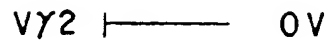


FIG. 6B

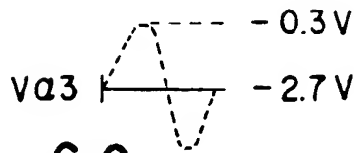


FIG. 6C

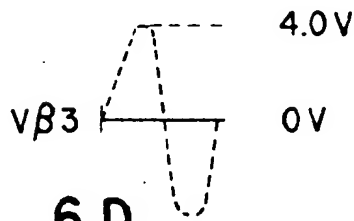


FIG. 6D

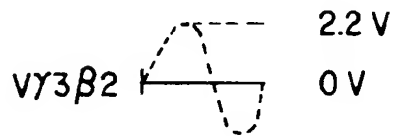


FIG. 6E

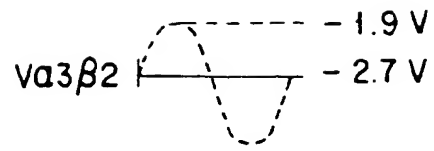


FIG. 6F

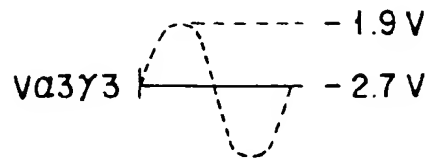


FIG. 6G

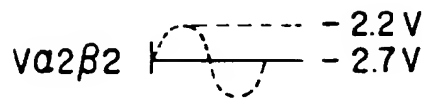


FIG. 6H

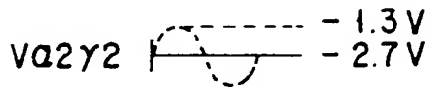


FIG. 6I

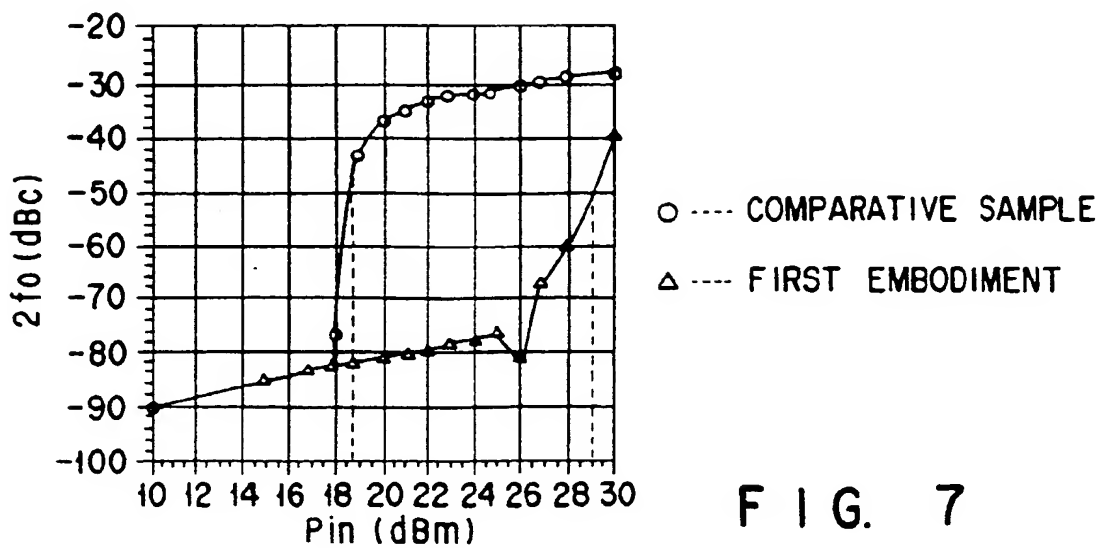


FIG. 7



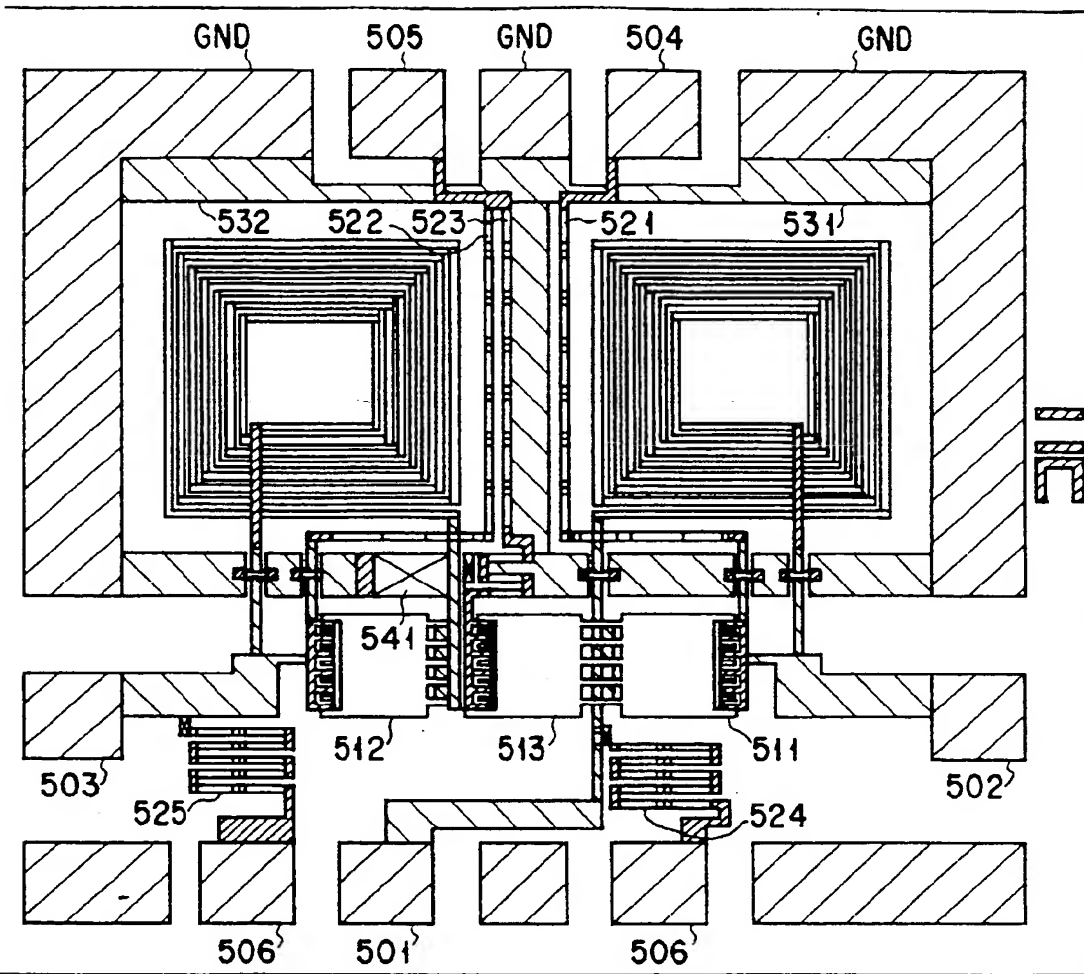


FIG. 8

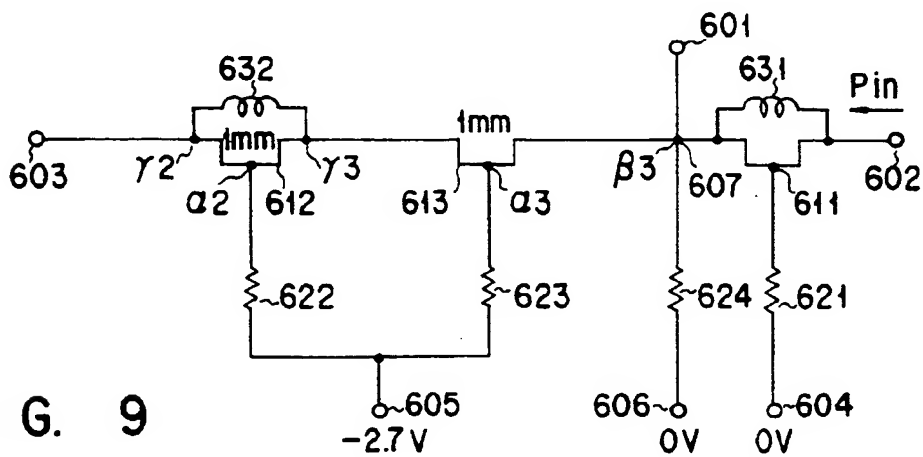


FIG. 9

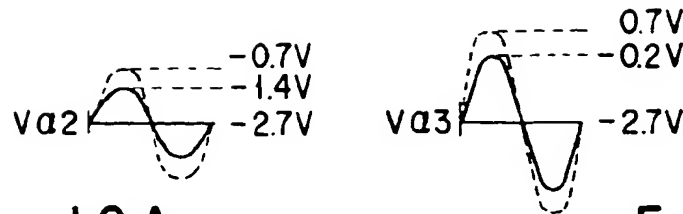


FIG. 10A

FIG. 10B

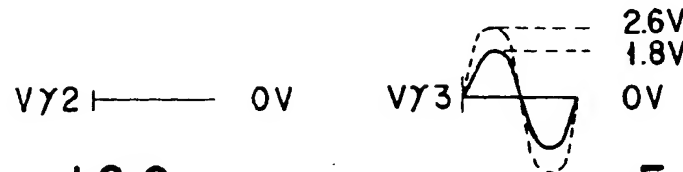


FIG. 10C

FIG. 10D

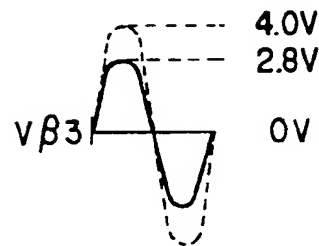


FIG. 10E

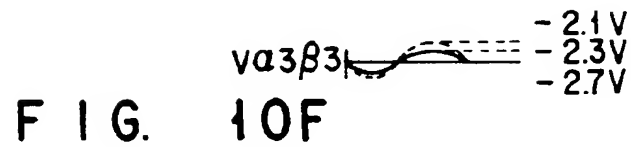


FIG. 10F

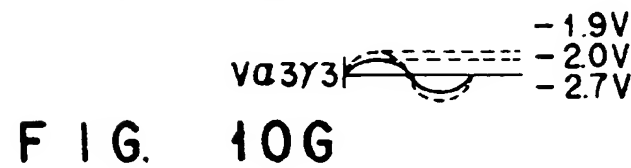


FIG. 10G

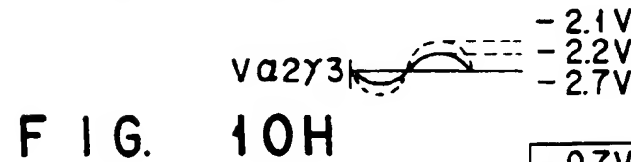


FIG. 10H

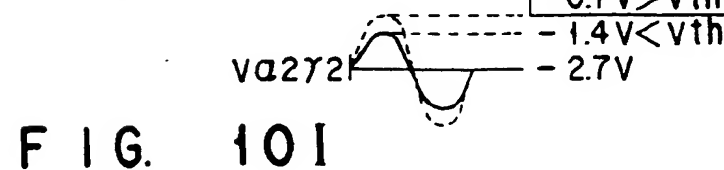


FIG. 10I

"ON" STATE AT  
Pin = 22dBm

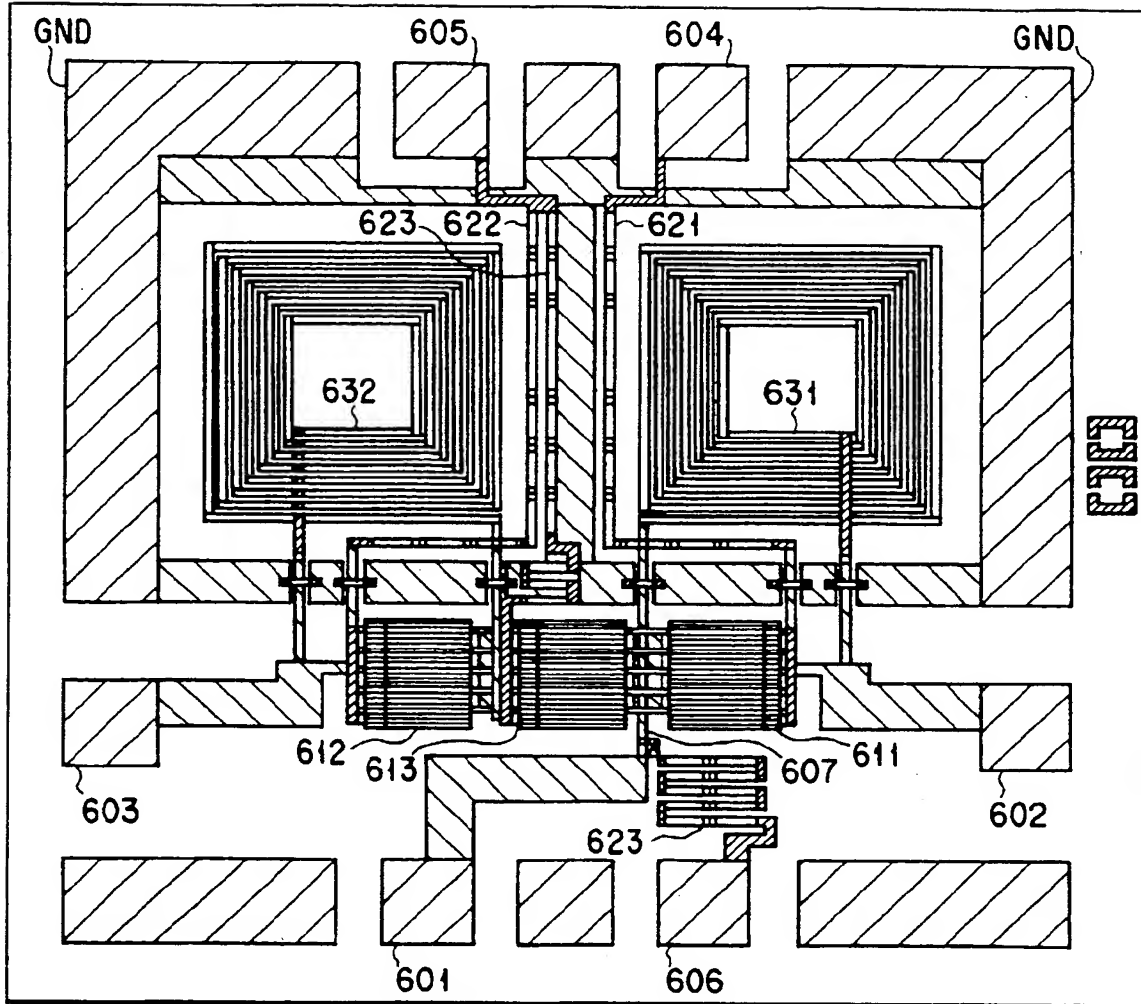


FIG. 11

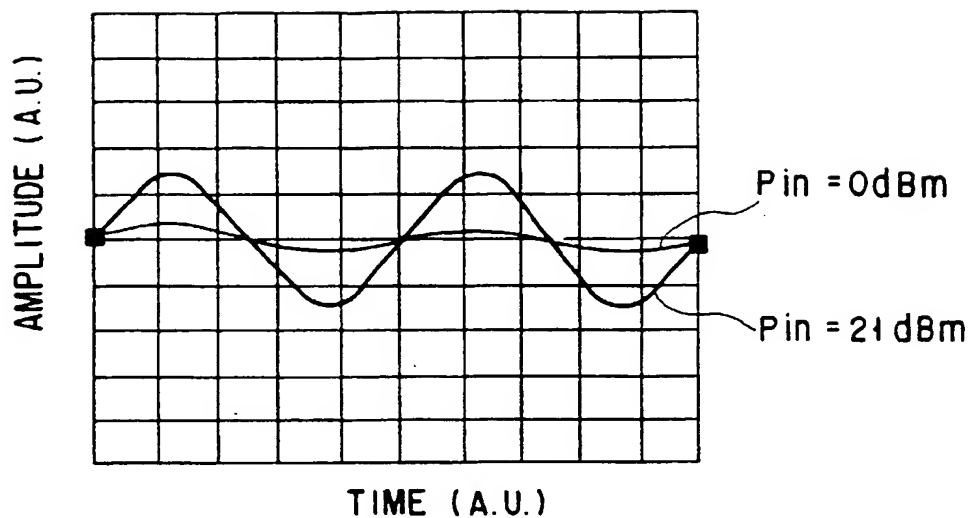


FIG. 12A

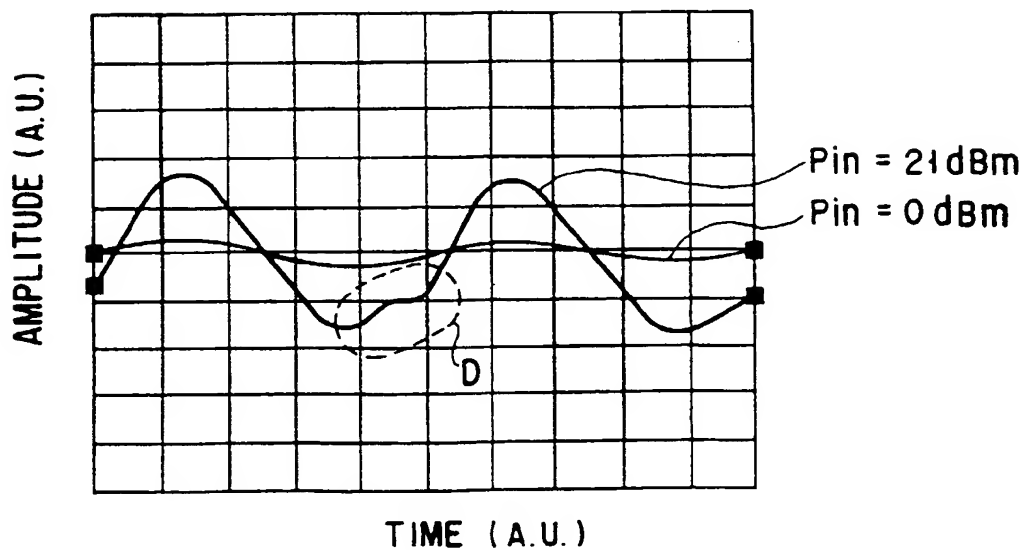


FIG. 12B

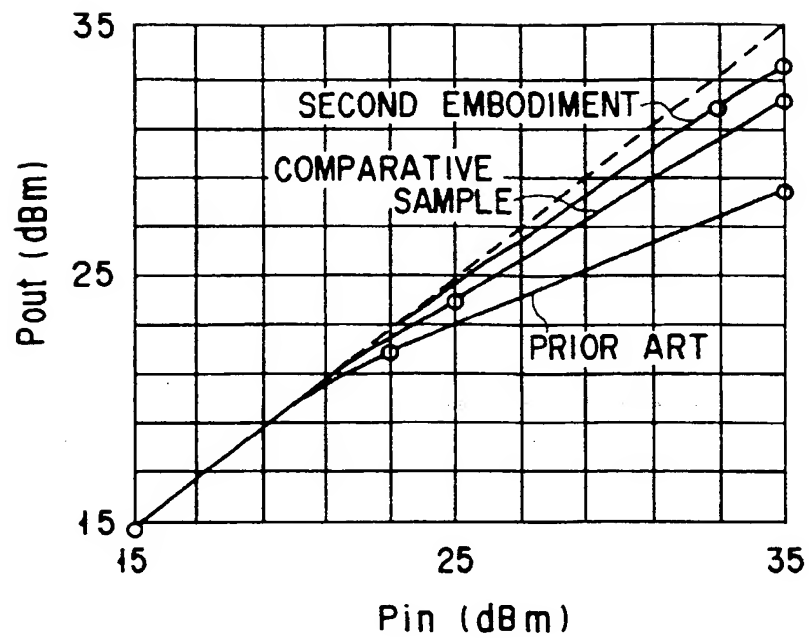


FIG. 13A

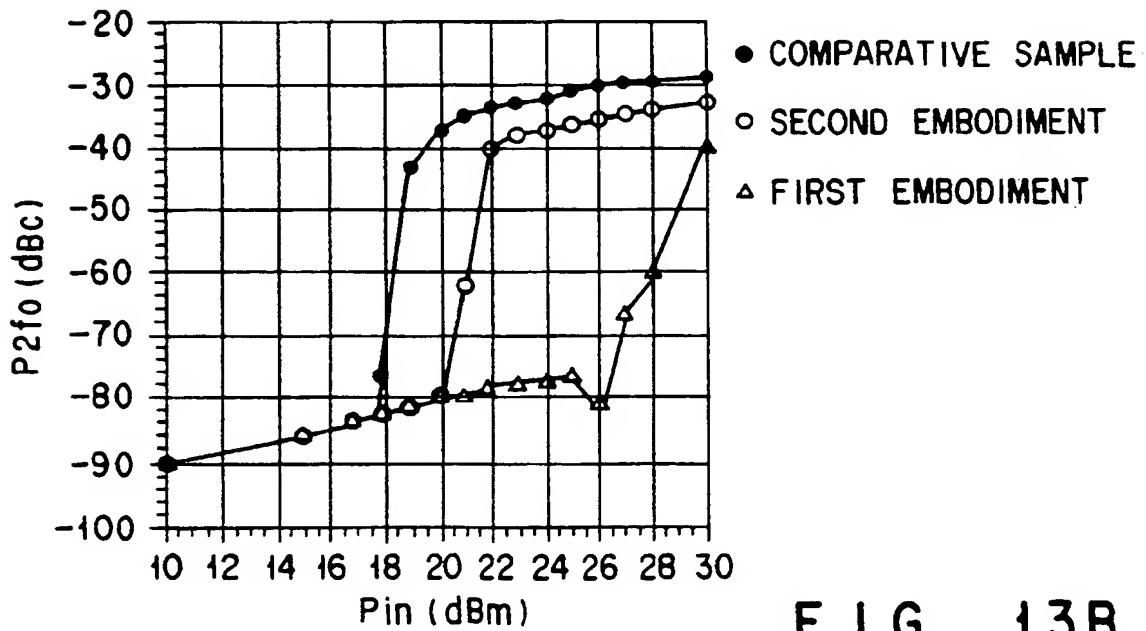


FIG. 13B

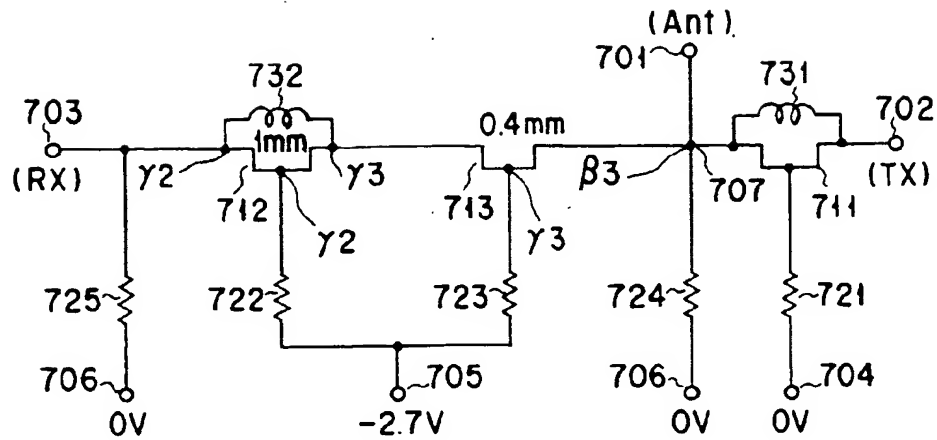


FIG. 14

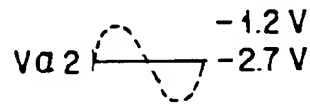


FIG. 15A

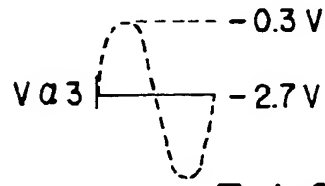


FIG. 15B



FIG. 15C

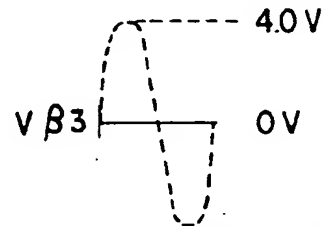


FIG. 15D

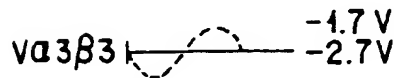


FIG. 15F



FIG. 15G



FIG. 15E

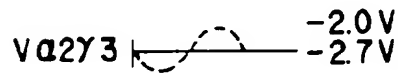


FIG. 15H



FIG. 15I

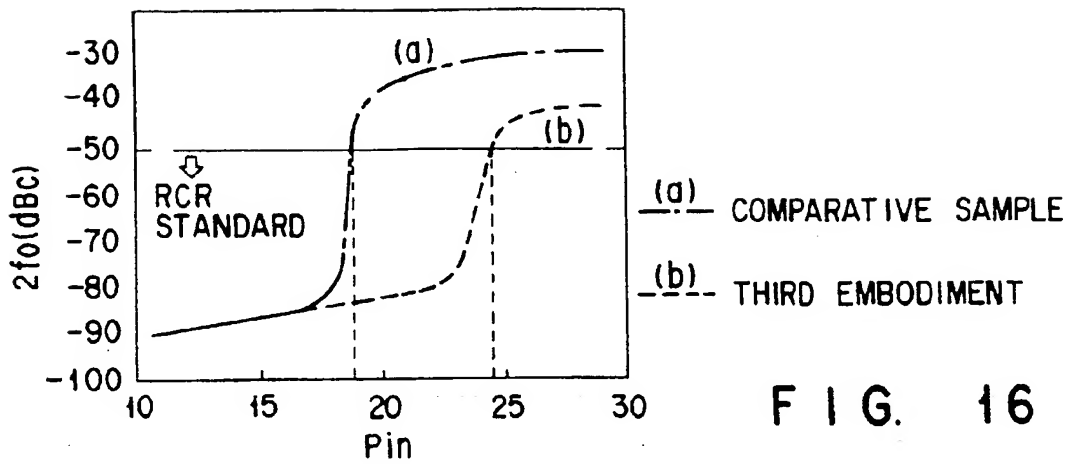


FIG. 16

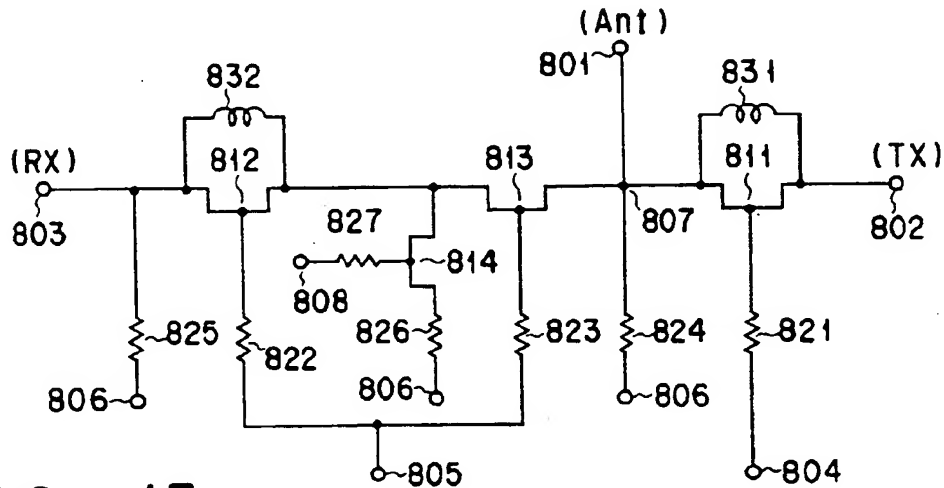


FIG. 17

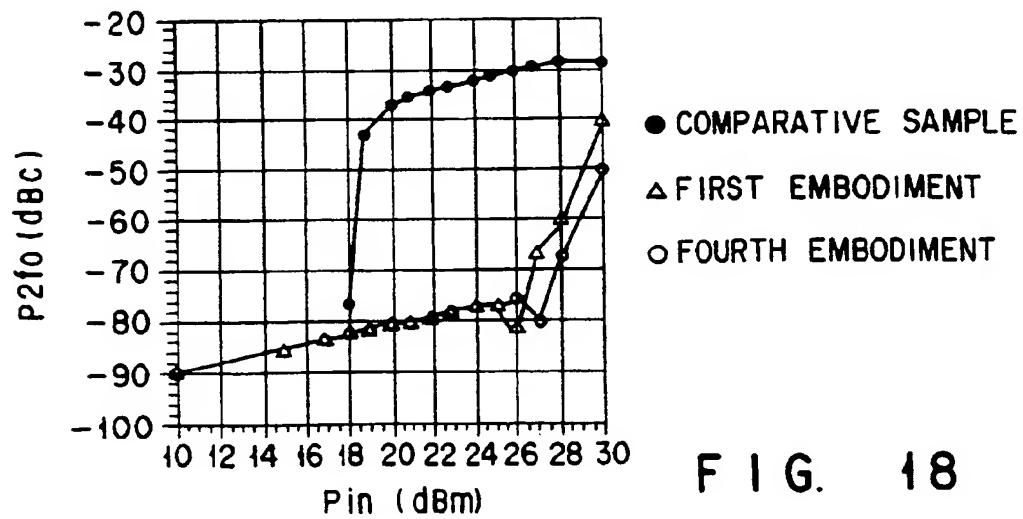


FIG. 18



(19)



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(12)

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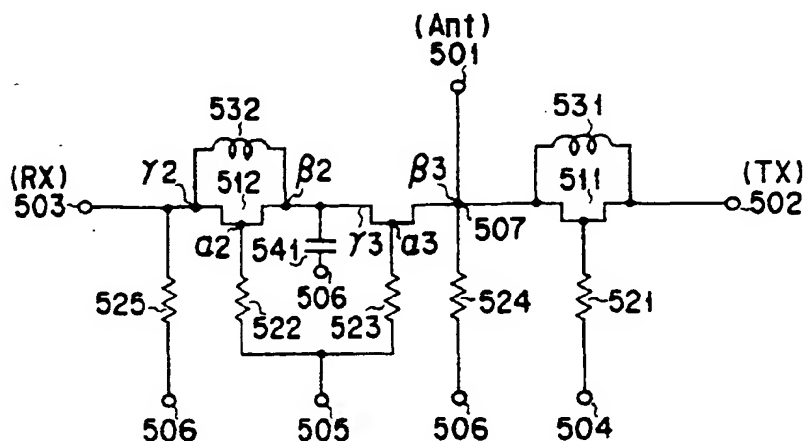
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**(54) Switching circuit**

(57) A switching circuit includes a first transmission path, a first input/output terminal (503) connected to one end of the first transmission path, a second input/output terminal (501) connected to the other end of the first transmission path, a second transmission path connected at one end to the second input/output terminal (501), and a third input/output terminal (502) connected to the other end of the second transmission path, wherein the first transmission path includes a first field effect transistor (512) having a first conduction path which is connected at one end to the first input/output terminal (503), a second field effect transistor (513) having a second conduction path which is connected at one end to the other end of the first conduction path of the first field effect transistor (512) and connected at the other end to the second input/output terminal (501), and a first inductor (532) connected in parallel with the first conduction path of the first field effect transistor (512).

sistor (512) having a first conduction path which is connected at one end to the first input/output terminal (503), a second field effect transistor (513) having a second conduction path which is connected at one end to the other end of the first conduction path of the first field effect transistor (512) and connected at the other end to the second input/output terminal (501), and a first inductor (532) connected in parallel with the first conduction path of the first field effect transistor (512).

**FIG. 5****EP 0 766 396 A3**



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# EUROPEAN SEARCH REPORT

Application Number  
EP 96 30 7074

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (InCl.6)
X	EZZEDDINE A ET AL: "A HIGH ISOLATION DC TO 18 GHZ PACKAGED MMIC SPDT SWITCH" PROCEEDINGS OF THE EUROPEAN MICROWAVE CONFERENCE, FOLKETS HUS, SWEDEN, SEPT. 12 - 16, 1988, no. CONF. 18, 12 September 1988, pages 1028-1033, XP000013544	1,2,15	H03K17/693 H01P1/15 H04B1/44
A	MICROWAVE EXHIBITIONS AND PUBLISHERS LTD * the whole document *	3-14, 16-20	
A	O'SULLIVAN P ET AL: "HIGH PERFORMANCE INTEGRATED PA, T/R SWITCH FOR 1.9 GHZ PERSONAL COMMUNICATIONS HANDSETS" PROCEEDINGS OF THE GALLIUM ARSENIDE INTEGRATED CIRCUITS SYMPOSIUM (GAAS IC), SAN JOSE, OCT. 10 - 13, 1993, no. SYMP. 15, 10 October 1993, pages 33-35, XP000462949 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * page 34, right-hand column - page 35, left-hand column; figure 5 *	11,17	
A	US 4 789 846 A (MATSUNAGA MAKOTO ET AL) 6 December 1988 * the whole document *	1-20	
A	MAKOTO MATSUNAGA ET AL: "HIGH-POWER MICROWAVE TRANSMIT-RECEIVE SWITCH WITH SERIES AND SHUNT GAAS FETS" IEICE TRANSACTIONS ON ELECTRONICS, vol. E75 - C, no. 2, 1 February 1992, pages 252-258, XP000301152 * the whole document *	1-20	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22 February 1999	Examiner Jepsen, J
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## EUROPEAN SEARCH REPORT

Application Number  
EP 96 30 7074

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	UDA H ET AL: "HIGH-PERFORMANCE GAAS SWITCH ICS FABRICATED USING MESFETS WITH TWO KINDS OF PINCH-OFF VOLTAGES" PROCEEDINGS OF THE GALLIUM ARSENIDE INTEGRATED CIRCUITS SYMPOSIUM (GAAS IC), SAN JOSE, OCT. 10 - 13, 1993, no. SYMP. 15, 10 October 1993, pages 247-250, XP000462982 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS		
A	SHIFRIN M ET AL: "MONOLITHIC CONTROL COMPONENTS HANDLE 27 W OF RF POWER" MICROWAVE JOURNAL, vol. 32, no. 12, 1 December 1989, pages 119-122, XP000116633		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>22 February 1999</b>	Examiner <b>Jepsen, J</b>
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